GAAS RFICS FOR CDMA/AMPS DUAL-BAND WIRELESS TRANSMITTERS

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ABSTRACT

An upconverter and two driver amplifiers for CDMA/AMPS cellular/PCS wireless transmitters are presented. The upconverter has two selectable RF outputs operating over 800 to 1900MHz frequency range. They can be assigned to different frequency bands providing a dual-band operation. The driver amplifiers offer two gain modes selected with a control voltage. The cellular driver amplifier provides DC power savings in the low gain mode. The chip set was fabricated using a GaAs 0.6um E/D MESFET process.

INTRODUCTION

The coexistence of cellular and personal-communications services (PCS) in the US demands dual-band mobile phones. Many service providers accepted the Code-Division Multiple Access (CDMA, IS-95A) technology offering improved phone performance and multifunctionality. However, CDMA handsets have to continue to support the analog AMPS technology as a fall-back standard in the areas where digital wireless service is not yet available.

Dual-band dual-mode handsets require transmitters capable of operation in both the cellular and PCS frequency bands. For dual-mode operation, the cellular portion of a transmitter must meet linearity requirements in CDMA mode and saturated power requirements in the FM mode. Reduction of output noise in the receive band is necessary for full duplex CDMA operation. This noise couples through the antenna duplexer to the receiver and can degrade sensitivity. Another requirement to mobile phone transmitters is the capability to operate from a low supply voltage with a low DC power consumption. Circuits powered directly off the battery should operate over a wide range of supply voltages.

This paper describes an upconverter and two driver amplifiers designed for dual-band dual-mode wireless transmitters. The circuits were fabricated using a GaAs 0.6um E/D MESFET process.

TRANSMITTER ARCHITECTURE

The block diagram of a dual-band transmitter using the designed upconverter and driver amplifiers is shown in Fig. 1. The upconverter receives the differential IF signal from a Tx AGC amplifier [1] followed by an IF filter with a differential output impedance of 265Ω. The upconverter has two single-ended broadband RF outputs operating over an 800 to 1900MHz frequency range. They can be assigned to different frequency bands providing a dual-band operation as shown in Fig. 1. The outputs are selected according to a control input based on the phone mode of operation. Each output is connected to a corresponding bandpass filter that attenuates the undesired sideband, LO leakage and the noise in the Rx band.

The cellular and PCS driver amplifiers operate in two gain modes selected with an external control voltage. This gain step is necessary to achieve the required dynamic range of CDMA transmitters. The driver amplifiers are followed by bandpass filters that provide further attenuation of the noise in the Rx band. Two outputs are provided for the PCS driver to allow the use of two narrow-band filters with a good attenuation in the Rx band. Each of these two filters covers only a portion of the PCS frequency band. The PCS driver outputs are activated according to a control input based on the carrier frequency.

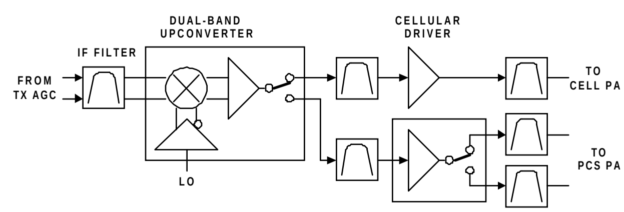

Fig. 1 Block diagram of a dual-band transmitter.

DUAL-BAND UPCONVERTER DESIGN

A schematic diagram of the upconverter is shown in Fig. 2. The mixer is implemented as a FET ring quad for lower intermodulation distortion [2, 3]. This mixer topology also exhibits good isolation between its ports and good spurious response rejection due to its double-balance nature.

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The postamplifier compensates for mixer losses and acts as an active balun converting the differential input to a single-ended output. The first stage of the postamplifier is a differential amplifier with a parallel resistive feedback that sets a broadband 265Ω input impedance of the upconverter. The drains of the differential MESFET pair are biased through resistors in series with inductors. The inductors compensate for the gain rolloff at PCS frequencies yielding a flat frequency response. The outputs of the differential stage are combined by a push-pull stage that also sets a broadband 50Ω output impedance. Both stages of the postamplifier provide common-mode rejection. The single-ended output of the postamplifier is split into the two upconverter outputs using an SPDT switch.

The LO buffer performs a 180° phase splitting and signal limiting. The phase splitter is implemented as a parallel combination of a common-source and common-gate stages. The common-gate stage also matches the LO port to 50Ω in a broad frequency range. The splitter is followed by an amplifier-limiter that boosts the voltage swing to the level required for reliable switching of the ring mixer FETs. The limiting function gives the desired amplitude balance and desensitizes the upconverter performance to the LO input power in a wide range.

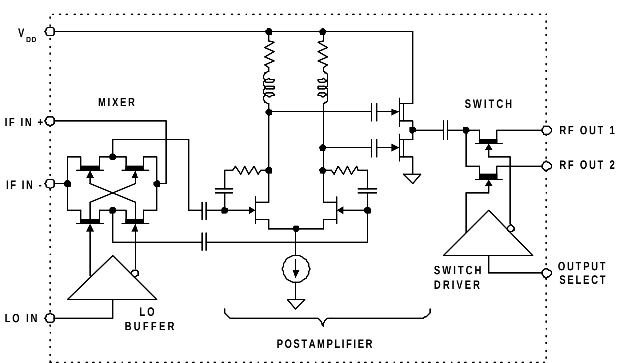

Fig. 2 Schematic Diagram of the Upconverter.

DRIVER AMPLIFIER DESIGN

Schematic diagrams of the cellular and PCS driver amplifiers are shown in Fig. 3 and 4 respectively. In the low gain mode, the output stage of the cellular driver is bypassed with an attenuator and powered down to provide DC power savings. The gain step in the PCS driver is realized by switching the shunt resistance of the second stage load. Each driver amplifier uses a parallel resistive feedback in the first stage that sets a 50Ω input impedance. The output is reactively matched to 50Ω using on-chip components. A single Vdd feed is used for all gain stages of each amplifier. The low-pass RC networks along the Vdd supply decouple the gain stages over a wide frequency range.

The gain stages of the amplifiers are biased for class-A operation to meet linearity requirements in CDMA mode. The cellular driver was designed to meet an additional requirement of saturated output power in FM mode. Both amplifiers were designed to operate from 3.4 to 5V supply voltage range.

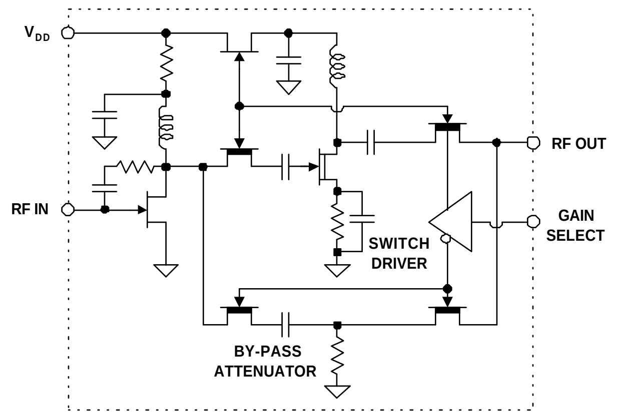

Fig. 3 Schematic Diagram of the Cellular Driver.

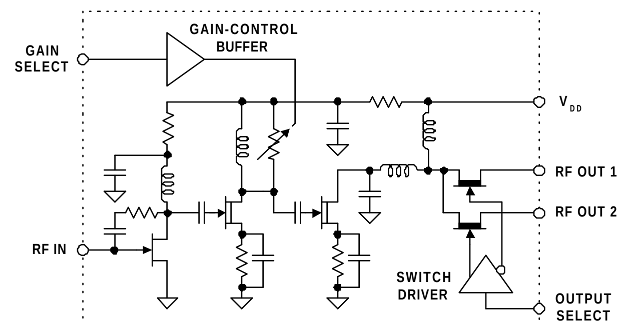

Fig. 4 Schematic Diagram of the PCS Driver.

A major design challenge for the PCS driver amplifier was achieving a stable high-gain operation in a small plastic package. Different packages were modeled using a technique described in [4]. An SSOP16 package with an exposed paddle was selected based on its superior isolation.

MEASURED PERFORMANCE

The upconverter was evaluated in a plastic SOIC8 package using a CDMA waveform as an input signal. The performance in the cellular and PCS frequency bands as a function of LO power and supply voltage is shown in Fig. 5 and 6 respectively. At P_{LO} of -6dBm and V_{DD} of 3.0V, the conversion loss is 0.5dB in the cellular band and 1.1dB in the PCS band. The noise figure is 11.5dB and 12.4dB respectively. The Adjacent Channel Power Rejection (ACPR) at P_{OUT} of -10dBm is better than 40dBc over a -10 to 0dBm LO power range and a 2.7 to 3.9V supply voltage range. Table 1 summarizes the room temperature performance of the upconverter.

The cellular driver amplifier was evaluated in SSOP16 package. The amplifier exhibits 22dB gain in high gain mode and 3dB loss in the low gain mode at V_{DD} of 3.4V. Fig. 7 shows the measured and simulated ACPR as a function of the output power in the high-gain mode. The ACPR was simulated using the AM-AM and AM-PM characteristics of the amplifier as described in [5]. The amplifier noise figure is lower than 3.4dB. Current savings in the low gain mode is more than 53%. The circuit preserves input and output match to 50Ω in both gain modes. The PCS driver was evaluated in SSOP16 package with an exposed paddle. The circuit demonstrated a stable high-gain operation for 10:1 input and output VSWR. Tables 2 and 3 summarize the room temperature performance of the driver amplifiers at 3.4 and 5.0V supply voltages.

CONCLUSIONS

An upconverter and two driver amplifiers were designed and fabricated for wireless applications. A broadband performance of the upconverter and the availability of two selectable RF outputs allow the use in dual-band transmitters, thus eliminating the need for two upconverters. The upconverter is capable of operation from 2.7V supply voltage with 21mA nominal current meeting the regulated power supply requirements of mobile handsets. The driver amplifiers can be biased directly off the battery and operate in a wide supply voltage range given by the battery over its lifetime. The cellular amplifier provides DC power savings in the low gain mode resulting in a higher efficiency of the transmitter at lower transmitted power. All the circuits demonstrate low noise figure required for low output noise power in the Rx band.

Although the RFICs were designed for cellular CDMA/AMPS and U.S. PCS wireless transmitters, they are versatile enough to be used in other applications such as GSM, the 900MHz ISM band and the Korean PCS band (1800MHz) transmitters.

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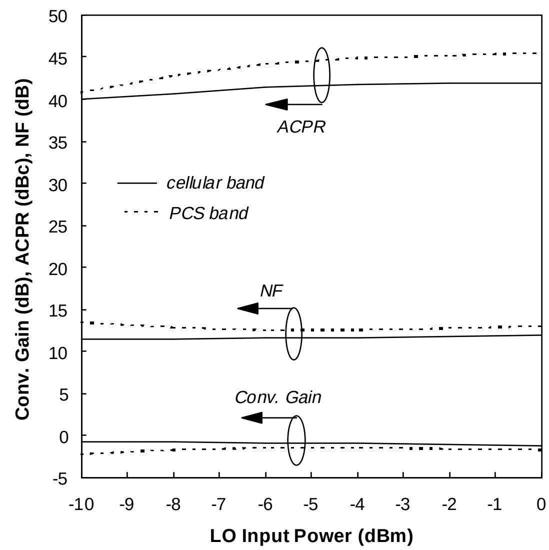

Fig. 5 Upconverter Performance as a Function of the LO Power (P_{OUT}=-10dBm, V_{DD}=2.7V).

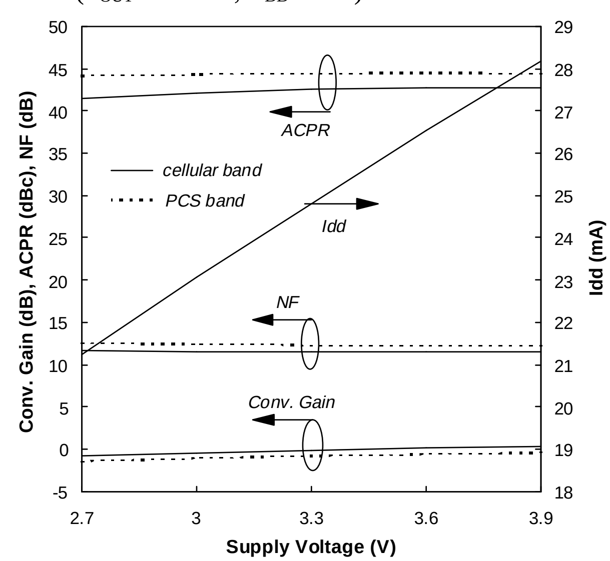

Fig. 6 Upconverter Performance as a Function of the Supply Voltage (P_{OUT}=-10dBm, P_{LO}=-6dBm).

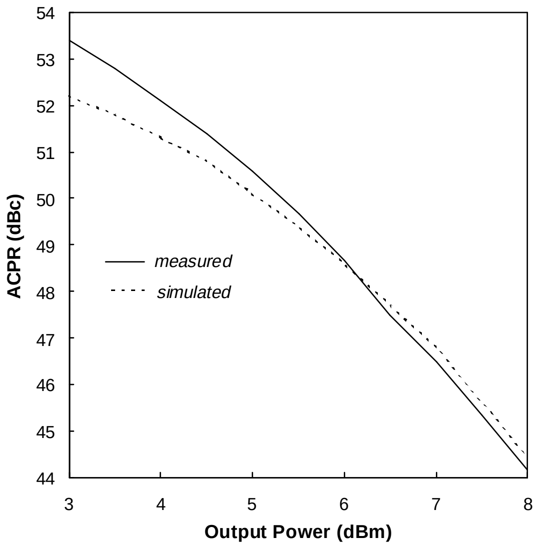

Fig. 7 Measured and Simulated ACPR of the Cellular Driver in High-Gain Mode at ±885kHz Offset (V_{DD}=5V).

RF Frequency (MHz)	**824-849**	**1850-1910**
LO Frequency (MHz)	**954-979**	**1620-1650**
Conversion Gain (dB)	**-0.5**	**-1.1**
Noise Figure (dB)	**11.5**	**12.4**
ACPR (dBc) @ P_{OUT}=-10dBm	**42.2 @ ±885kHz**	**44.3 @ ±1.25MHz**
P_{OUT} (dBm) @ 1dB Compression	**-1.2**	**-1.3**
LO to RF Leakage (dBm)	**-31.6**	**-25.7**
I_{DD} (mA)	**22.3**	**23.1**

Table 1. Upconverter Performance summary (V_{DD}=3V, P_{LO}=-6dBm).

V_{DD} (V)	**3.4**	**5.0**
High / Low Gain (dB)	**22.0 / -3.0**	**23.5 / -2.2**
HG / LG ACPR (dBc) @ ±885kHz Offset & P_{OUT}=+3 / -22dBm	**47 / 55**	**53 / 55**
HG P_{OUT} (dBm) @ 1dB Compression	**11**	**14**
HG / LG NF (dB)	**3.4 / 6.0**	**3.3 / 5.8**
Input VSWR	**1.4**	**1.5**
Output VSWR	**1.4**	**1.4**
HG / LG I_{DD} (mA)	**31.5 / 12.5**	**47 / 22**

Table 2. Cellular Driver Amplifier Performance Summary.

V_{DD} (V)	**3.4**	**5.0**
High / Low Gain (dB)	**28.1 / 5.1**	**30.5 / 7.4**
HG / LG ACPR (dBc) @ ±1.25MHz Offset & P_{OUT}=+10.5 / -14.5dBm	**38.1 / 37.0**	**42.5 / 44.2**
HG / LG NF (dB)	**4.4 / 7.5**	**3.8 / 6.4**
Input VSWR	**1.4 / 1.7**	**1.4 / 1.6**
Output VSWR	**1.6 / 1.7**	**1.8 / 1.9**
HG / LG I_{DD} (mA)	**36.0 / 36.0**	**50.0 / 50.0**

Table 3. PCS Driver Amplifier Performance Summary.